SMC-01-1507

December 10, 2003

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/661,745 09/14/03

Chia-Ta Hsieh

A TRAPEZOID FLOATING GATE TO IMPROVE PROGRAM AND ERASE SPEED FOR SPLIT GATE FLASH

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December 19, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 12/19/03

U.S. Patent 5,723,371 to Seo et al., "Method for Fabricating a Thin Film Transistor Having a Taper-Etched Semiconductor Film," teaches a method for fabricating a thin film transistor having a taper-etched semiconductor film, where the sharpness of corners is reduced.

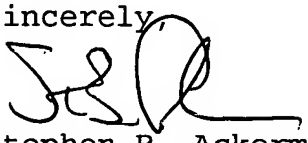
U.S. Patent 5,728,259 to Suzawa et al., "Process for Fabricating Thin-Film Semiconductor Device Without Plasma Induced Damage," discloses a process for tapered silicon films in a method of fabricating a semiconductor device in which a gate insulating layer has no plasma induced damage.

U.S. Patent 6,228,695 to Hsieh et al., "Method to Fabricate Split-Gate with Self-Aligned Source and Self-Aligned Floating Gate to Control Gate," discloses a split-gate flash memory cell with self-aligned source and self-aligned floating gate to control gate.

U.S. Patent 6,259,131 to Sung et al., "Poly Tip and Self Aligned Source for Split-Gate Flash Cell," discloses a method of forming a polysilicon gate tip in split-gate flash memory cells for enhanced F-N tunneling.

U.S. Patent 5,393,682 to Liu, "Method of Making Tapered Poly Profile for TFT Device Manufacturing," discloses a method for making tapered polysilicon gates.

Sincerely,



Stephen B. Ackerman,
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Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
TSMC-01-1507	10/661,745
Applicant: Chia-Ta Hsieh	
Filing Date: 09/12/03	Group Art Unit:

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6259131	7/10/01	Sung et al.	257	315	5/27/98
	5393682	2/28/95	Liu	437	41	12/13/93
	5723371	3/3/98	Seo et al.	438	158	8/23/95
	5728259	3/17/98	Suzawa et al.	156	646.1	10/19/95
	6228695	5/8/01	Hsieh et al.	438	201	5/27/99

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.